A 900MHZ ISM BAND TRANSCEIVER RF IC CHIP SET AND RF MODULE

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ABSTRACT

This paper demonstrates a packaged RF front-end IC chip set (transmitter and receiver) and a highly integrated transceiver RF module used in the 902~928MHz ISM band. By using the RF IC chip set with other application circuits, this module can provide the sensitivity of -93dBm at 1.152Mb/s data rate. The transmit power of the module can be varied continuously from -10dBm to +20dBm simply by a 0~3V DC control voltage. The average current consumption of the module under TDD operation is 150mA for +20dBm output power, and 60mA for -10dBm output power.

INTRODUCTION

This paper describes a packaged transceiver RF front-end IC chip set and a small size RF module used in 902~928MHz ISM band. Figure 1 shows the block diagram of this RF module, which is used for direct-sequence spread spectrum (DSSS) operation. The RF IC chip set, comprised of two ICs (transmitter and receiver), are fabricated in a GaAs 1-um ion-implant E/D MESFET process and fitted in plastic SSOP packages. The receiver IC includes an antenna switch, a low noise amplifier, and a mixer. The transmitter IC is mainly a power amplifier with a negative bias generator and a continuous power control circuit.

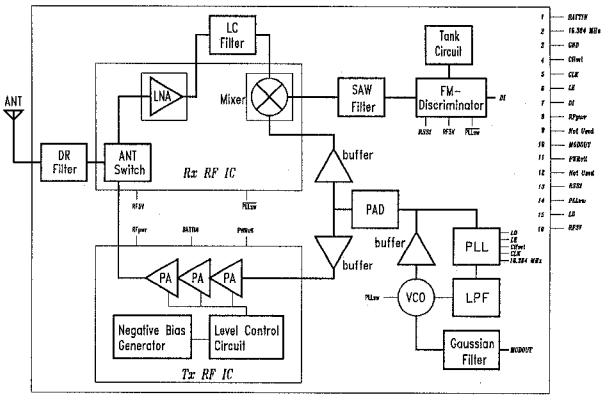

Figure 1. Block diagram of the RF module

THE RECEIVER IC

The receiver RF IC, packaged in a 24-pin plastic SSOP, consists an antenna switch, a low noise amplifier (LNA), and a mixer. Figure 2 shows the photograph of the receiver IC. The more detail circuit topology and performance are described as follows.

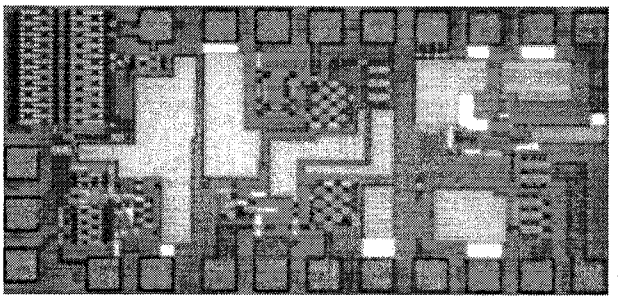

Figure 2. The receiver IC photograph

The antenna switch is an SPDT switch constructed by MESFETs. After packaging,

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the insertion losses are below 1dB for both Tx and Rx branches, and the return loss is better than 20dB in each port (Figure 3). Besides, the isolation from Tx port to Rx port is about 30dB. The 1-dB gain compression point is about +28.2dBm, however, the Tx mode insertion loss will not increase until the Tx power is over +25.2dBm.

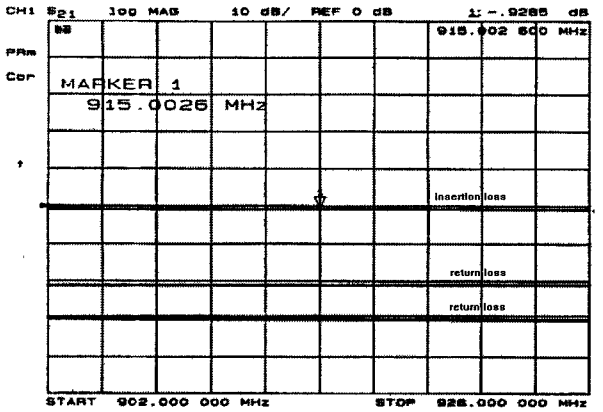

Figure 3. Insertion loss and return loss of the antenna switch

The low noise amplifier has three stages. The first two stages are cascoded MESFETs which are then cascaded with a common-source amplifier. Large source inductors are added to each stage, such that the performance is compromised between the noise figure, return loss, and stability. To stabilize the DC supply current, an active bias circuit is designed to prevent from the process variation. After packaging and external impedance matching, typical noise figure is 1.2dB and gain is 24dB (Figure 4) with return loss better than 14dB. Its output 1-dB gain compression point is 0dBm. The current consumption for the LNA is 10mA at 3V voltage supply. If the supplied voltage is reduced to 2.3V, the noise figure and gain will degrade 0.2dB and 2.8dB respectively, while the current consumption will be reduced to 6mA.

The mixer is composed of two cascoded DFETs. The RF signal is applied to the gate of the bottom DFET. After passing through a common-gate buffer, the LO signal is injected to the gate of the upper DFET. With 0dBm LO power injection, typical conversion gain and single side band (SSB) noise figure is 8.5dB and 7.5dB respectively (Figure 5). The return loss of each port is better than 10dB and the output 1-dB gain compression point is 0dBm. Current consumption of the mixer is about 10mA at 3V voltage supply.

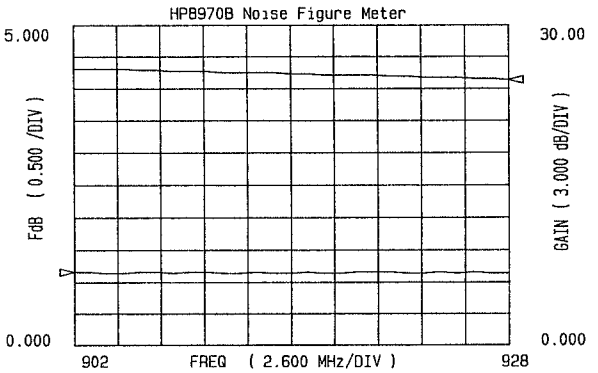

Figure 4. LNA gain and noise figure

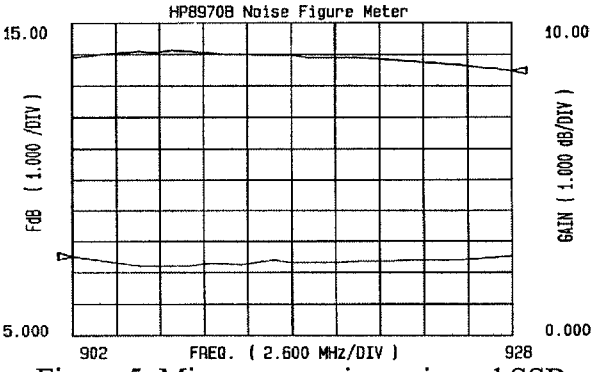

Figure 5. Mixer conversion gain and SSB noise figure

The conversion gain and NF of the receiver IC is about 32dB and 2.3dB respectively under the bias condition of 3V/20mA. If a DR filter and an image rejection LC filter are included, the overall conversion gain and NF of the receiver front-end will be 24dB and 3.6dB respectively (Figure 6).

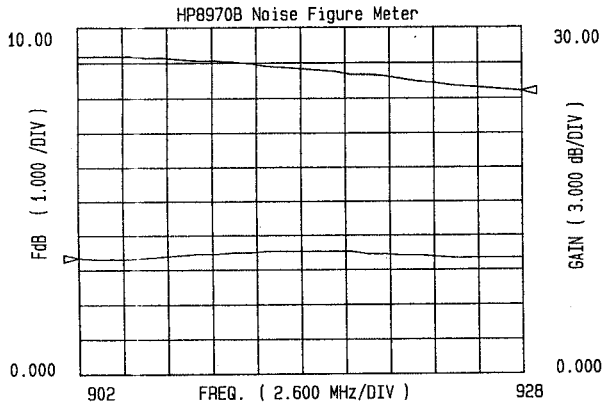

Figure 6. Conversion gain and noise figure of the receiver front-end

THE TRANSMITTER IC

The transmitter RF IC, packaged in a 28-pin plastic SSOP, includes a three-stage power amplifier (PA), a negative bias generator (NBG), and a power control circuit (PCC). Figure 7 shows the photograph of the transmitter IC.

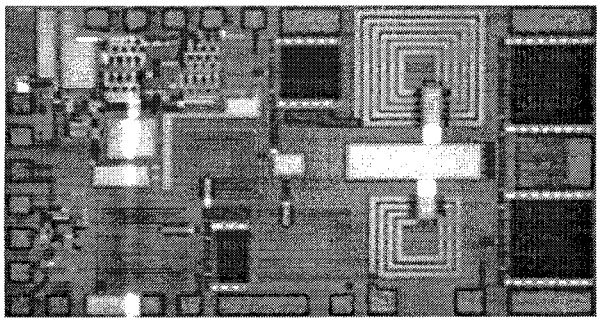
Figure 7. The transmitter IC photograph

The NBG has a voltage conversion efficiency of 99% (no load current), and it's power efficiency is about 90%. Furthermore, the NBG output load resistance is about 85 ohms and the oscillating frequency is 480kHz. As to the power control circuit, a 0~3V DC input control signal is used to control the output power of the PA with a control apparatus.

As a result, the transmitter IC can deliver power from -10dBm to over +23dBm with -3dBm input power level and the current consumption is from 10mA to 170mA at 3.3V voltage supply (Figure 8). In nominal case, the total efficiency (including the current of NBG, PCC, PA and the external power down switch) of this transmitter RF IC is about 40%. In addition, it can also be tuned to have +25.5dBm output power, and consume only 240mA at 3.3V. When 5V voltage is applied, the output power can be greater than +29dBm, and the efficiency is up to 48% with total current consumption of 335mA at -2dBm input power.

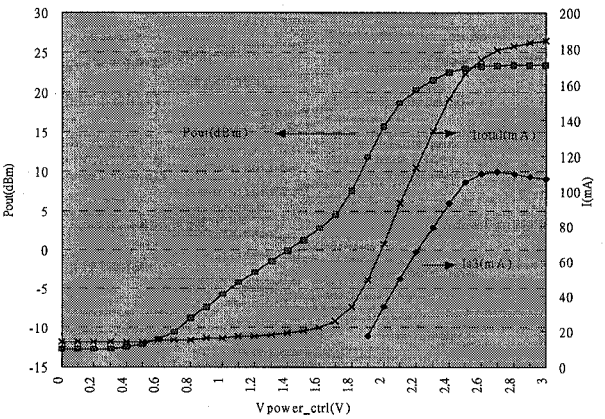

Figure 8. PA output power(Pout) & DC current(Itotal) vs. control voltage(Vpower_ctrl)

THE RF MODULE

The RF module, shown in Figure 1, consists of the receiver front-end, the transmitter, a demodulator and a frequency synthesizer.

As for the synthesizer in the TDD system, fast settling time and low phase noise are both required. A dual band voltage-controlled oscillator (VCO) is used to generate the T/R frequencies by changing the inductance of the resonator, thus reduces the cost and still maintains fast settling time. Typical phase noise of the synthesizer is better

than -100 dBc/Hz at 100kHz offset with 0dBm output power, and the frequency settling time is less than 200uS within 10kHz of the final frequency.

At the transmitting mode, baseband data with data rate of 1.152Mb/s, filtered by the Gaussian filter (BT=0.5), is modulated by the synthesizer to generate the GFSK signal, then amplified by the PA IC to transmit. The overall RF module can transmit power from -10dBm to +20dBm continuously just by a 0~3V DC control voltage.

At the receiving mode, RF signal received by the antenna goes through a DR filter, the receiver IC, a SAW filter and the demodulator. It can provide the sensitivity of -93dBm @10E-3 BER (Figure 9).

Under the TDD operation, average current is 150mA for +20dBm output power and 60mA for -10dBm output power. All of the elements of the RF module are mounted on single side of the PCB. The dimension of the module is 4.5cm by 6.3cm by 0.56cm. Figure 10 shows the photograph of this RF module.

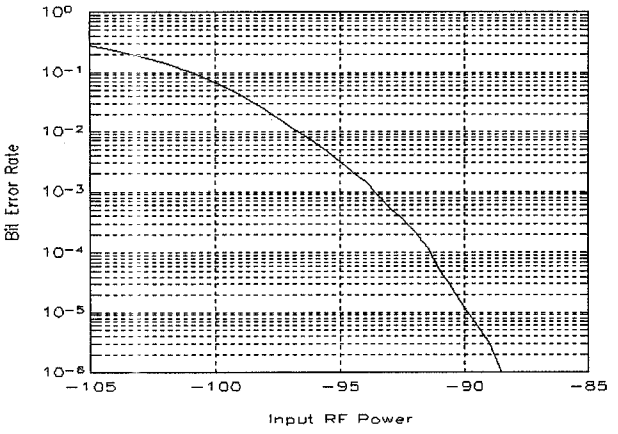

Figure 9. BER test result of the RF module (RF: 915MHz; data rate: 1.152Mb/s)

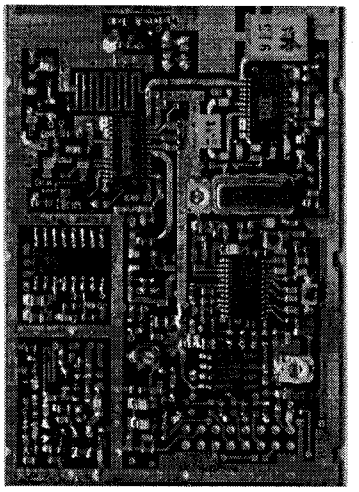

Figure 10. The photograph of the RF module (size: 4.5cm × 6.3cm × 0.56cm)

CONCLUSION

A 900MHz ISM band GaAs RF IC chip set and RF module have been successfully developed. The RF IC chip set includes a transmitter IC and a receiver IC. Measured performance of each IC was presented. The RF module can provide the sensitivity of -93dBm at 1.152Mb/s data rate, and transmit over 0.1W power. The output power of the module can also be varied continuously from -10dBm to +20dBm simply by a 0~3V DC control voltage. The average current consumption of the module under TDD operation is 150mA for +20dBm output power, and 60mA for -10dBm output power.

REFERENCES

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[2] Jack Browne, "Low-Power Chip Set Simplifies 900-MHz Cordless Designs," Wireless System Design, pp. 52-53, Jan., 1996.